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13. ABSTRACT (Maximum 200 words) Quantum mechanical devices utilize the wave nature of electrons for their operations whenever the electron mean-free-path exceeds the appropriate dimensions of the device structure. Some of the issues such as the tunneling time, the reduction of the dielectric constant and the drastic increase in the binding energy of dopants were studied. In the past several years, certain schemes appeared which may facilitate the realization of silicon quantum devices, such as the resonant tunneling via nanoscale silicon particles imbedded in an oxide matrix, and the superlattice barrier for silicon consisting of several period of Si/O. Epitaxially grown silicon beyond the superlattice barrier region, consisting of Si/adsorbed oxygen is free of stacking fault defects, and thus is potentially important for silicon based quantum devices. We have succeeded in fabricating an electroluminescent diode, which was life-tested for more than eight months without degradation. We have built a Si/O barrier structure with epitaxial silicon on top of the barrier as possible replacements for SOI (silicon on insulator), which should promote the effort in high speed and low power MOSFET devices. Our success may have opened the door for an electronic and photonic chip of the future ICs.				
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TECHNICAL FINAL REPORTS: STUDIES OF SILICON NANOCRYSTALS

30541-EL, April 1, 1993 to February 28, 1998, DAAH04-93-G-0067

Raphael Tsu, University of North Carolina at Charlotte

1. BRIEF OUTLINE OF RESEARCH FINDINGS AND ACCOMPLISHMENTS

Under the ARO supports, we have advanced a number of fundamental understandings in the world of man-made quantum phenomena, these includes:

- Quantum confinements in nanoscale silicon particles embedded in an oxide matrix and the observation of resonant tunneling via the nano-particles
- Quantum effects in a layer bounded by a heterojunction and a surface
- Quantum nature of Porous silicon. The studies on porous silicon for optoelectronic applications were terminated after the discovery of insurmountable difficulties with the poor morphology of porous silicon.
- Theoretic models of dielectric constant, doping, capacitance and excitons in Si nano-particles.
- Visible Light emission in Si nanoparticles, both in Porous Si and in an oxide matrix.
- Epitaxial barrier in silicon: with multi layers of Si/adsorbed oxygen. The discovery of silicon epitaxy free of stacking fault defects beyond the disordered monolayer of adsorbed oxygen has provided the basis of Si/O barrier for silicon quantum devices. A 2-period structure shows an effective barrier height of 0.5eV, sufficient for most silicon quantum devices at room temperature. The structure may be used to replace silicon on insulator (SOI) for high speed, low power transistors of the future.
- An electroluminescent diode structure consisting of a 9 period of Si (1.1nm) / monolayer of adsorbed oxygen superlattice shows visible light with a peak at 2.2eV life-tested for more than 8 months without any observable degradation.
- The extension to other gas species such as Si/C , Si/N ,etc. will be explored with our existing ARO grant.
- The time for thinking of an all silicon optoelectronic device is at hand-an electronic and photonic superchip.

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2. Table of Contents

Final progress Report

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A Special Report based on a Chapter in IJHSES-World Scientific,
Singapore, edited by M. Dutta and M. Strosio

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4. Statement of the problem studied

Quantum mechanical devices utilize the wave nature of electrons for their operations whenever the electron mean-free-path exceeds the appropriate dimensions of the device structure. Some of the issues such as the tunneling time, the reduction of the dielectric constant and the drastic increase in the binding energy of dopants are discussed. In the past several years, certain schemes appeared which may facilitate the realization of silicon quantum devices, such as the resonant tunneling via nanoscale silicon particles imbedded in an oxide matrix, and the superlattice barrier for silicon consisting of several period of Si/O. This report is to show that dielectric breakdown can occur under fabrication condition without using a controlled forming process. Epitaxially grown silicon beyond the superlattice barrier region, consisting of adsorbed oxygen is free of stacking fault defects, and thus is potentially important for silicon based quantum devices, including electroluminescent diodes, as well as serving as an SOI (silicon on insulator). The replacement of SOI by the epitaxially grown Si/O superlattice barrier should promote the effort in high speed and low power MOSFET devices.

5. Summary (also see 1.)

Speed and density go together : scaling down the device size leads to higher speed and density. How far can scaling go? Operating voltages are set by the thermal voltage. Reducing size results ultimately to highfields beyond the breakdown. Besides, quantum effects will be reached at some point. These effects are not all desirable, for example, quantum interference is too size dependent, demanding unrealistic manufacturing tolerances. As the size approaches few nm, it is even impossible to dope due to the drastic increase in the binding energy of dopants. Classically, one talks about storing charges, as we have seen that quantum mechanically, one can only confine charges with a barrier. And electrons and holes confined in a barrier do leak out. Surely one can use thicker barrier to reduce tunneling, then, it is not possible to quickly remove the confined particle unless a large barrier lowering field is applied. The problem with this scheme is that one needs to localize the applied field, otherwise many adjacent structures will be affected. What is needed is judicious applications of quantum effects far from the notion that quantum transistors must be better! Fortunately, what is focussed in this report is not about wide spread utilization of quantum confinement. Rather, in some specific applications, for example, (a) the epitaxial Si/O superlattice for replacing the SOI fabricated by ion-implantation, (b) fabrication of a RTD in silicon, (c)

increasing the oscillator strength of silicon by quantum confinement for optoelectronic purposes, and (d) discretizing the I-V as resonant tunneling via nanoscale particles for multistage logic and functional devices. After stating all that, I am impelled to be optimistic that a totally new system fully utilizing the wave nature of quantum mechanics is right around the corner, waiting to be explored, even in silicon. The task at hand is huge, therefore, it is important to sort out those goals which can be successfully pursued with the available funding, to arrive at some consensus among the researchers for future endeavors.

6. Publications

For a coherent picture , the publication list includes those under ARO support or partial support previous to the present contract starting April 1,1993

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7. **List of Participants (Including those supported by previous ARO grant, also some of those listed were supported for only part of the grant period)**

Postdoctoral fellows

- Dr. Q. Zhang Post-doctoral fellow, Feb. 1997-present (1/2)
 Dr. Jinli Ding Post-doctoral fellow, Feb. 1995- Mar. 1998(1/2), now at U. Toronto
 Dr. Davorin Babic Post-doctoral fellow, Feb. 1991-Sept. 1994 (1/2), now at U. Illinois

Dr. Qui Yi Ye Post-doctoral fellow, Jan. 1990- May 1992 (1/4), now at IBM/Siemans
Dr. F. Zipman Post-doctoral fellow, Aug. 1988-Feb. 1990 (1/4), now at U. Puerto Rico

Students

A. Filios Ph.D. Candidate, Fall 1998(1/2), MS 1995
J.Dinkler MS Fall 1998 (1)
F. de Freitas MS candidate , April 1998 – present (1)
C. Lofgren MS 1993, Ph.D. Candidate Joint NC-State/UNCC program (1/4)
D. Boeringer, MS May 1994 (1/4) now at Grumman
J. Morias Ph.D. April 1996 UNICAMP,Brazil (thesis performed at UNCC), (1/4)
A. Bowhill MS August 1994 (1/2), now at Cirrus
C. Ding MS August 1995 (1/2)

8. Reports of Inventions:

None at this time

STUDIES OF SILICON NANOCRYSTALS: A final report

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Quantum mechanical devices utilize the wave nature of electrons for their operations whenever the electron mean-free-path exceeds the appropriate dimensions of the device structure. Some of the issues such as the tunneling time, the reduction of the dielectric constant and the drastic increase in the binding energy of dopants are discussed. In the past several years, certain schemes appeared which may facilitate the realization of silicon quantum devices, such as the resonant tunneling via nanoscale silicon particles imbedded in an oxide matrix, and the superlattice barrier for silicon consisting of several period of Si/O. This report is to show that dielectric breakdown can occur under fabrication condition without using a controlled forming process. Epitaxially grown silicon beyond the superlattice barrier region, consisting of adsorbed oxygen is free of stacking fault defects, and thus is potentially important for silicon based quantum devices, including electroluminescent diodes, as well as serving as an SOI (silicon on insulator). The replacement of SOI by the epitaxially grown Si/O superlattice barrier should promote the effort in high speed and low power MOSFET devices. The task at hand is huge, therefore, it is important to sort out those goals which can be successfully pursued with the available funding, to arrive at some consensus among the researchers for future endeavors.

1. Introduction

The use of heterojunctions for the confinement of carriers initiated the man-made quantum devices.^{1,2} Basically, whenever the electron mean-free-path exceeds the appropriate device dimension, the wave nature dominates. An excellent review by Cahay and Bandyopadhyay discussed in detail the implications and consequences of electrons and holes dictated by the wave nature, the granularity of charges and the polarization of spins.³ Several issues, such as the capacitance, the binding energy of dopants, and tunneling time, are reviewed in this report. The use of nanoscale silicon particles imbedded in an oxide matrix was introduced^{4,5} for possible silicon quantum devices operated at room temperature. A diode structure with annealing and oxidation of a thin amorphous silicon layer sandwiched between oxide layers, followed by a proper electrical forming process,⁶ was initially chosen for studies. It is noted that electrical forming is essential for the minimization of possible breakdown with high electric field,⁷ as well as serving as a selection of particle sizes. The evidences of resonant tunneling via nanoscale silicon imbedded in an oxide matrix are presented. In the last section, recent results in building a barrier consisting of alternate monolayers of oxygen sandwiched between adjacent thin silicon layers,^{8,9} are summarized. A barrier consisting of several periods of Si/O shows excellent isolation. Silicon growth beyond the barrier region is epitaxial and free of stacking fault defects. This represents a step in the right direction for the fabrication of quantum silicon devices as well as for the replacement of SOI¹⁰ in high speed and low power silicon MOSFET devices of the future. An all silicon electroluminescent device consisting of Si/O superlattice shows a peak at 2.2eV lasting more than eight months without degradation. The advent of a "superchip", electrons and photons are at hand.

1.1. Tunneling Time in a Quantum Well

There appears to be some inconsistency in the description of tunneling time. Cahayet al ¹¹ shows a pronounced dip in the tunneling time at the quasi-bound state (resonant state), whereas, the phase-delay time is a maximum at this energy.¹² Several approaches ¹³ were used including solving the time dependent Schroedinger equation with prescribed initial conditions, specifying a wavepacket and calculating the time it takes to traverse the double barrier structure.¹⁴ Results show that the tunneling time of a Gaussian packet from the time-dependent solution is very close to the phase-delay time. Figure 1 shows the comparison for various descriptions for a DB (double barrier) structure with well width of 6nm, barrier width of 2.5nm and barrier height of 0.3eV, and $m^*/m = 0.67$. The solid line shows the computed result using ¹³

$$\tau = d\phi / d\omega \quad (1)$$

where $\phi = kd + \theta$, is the total phase shift, with θ being the phase of the transmission coefficient, and d , the length of the DB structure. Note that the delay time peaks at resonances. The two small circles are values obtained from multiplying $\tau_0 = d / (hk/2\pi m^*)$ by $Q = E / \Delta E$, with ΔE the line-width at resonance. These results are quite easy to understand, resonances are produced by a wave bouncing back and forth for a number of cycles determined by the quality factor of the resonant system. This time is the standard delay time. Now, we want to show that tunneling time given by the time for a wavepacket traverses the structure using the solution of the time dependent Schroedinger equation gives essentially the same results, as shown in Fig. 1 : dashed and dash-dot for the build up time and decay time for the charges inside the quantum well respectively; and the time of traversing for a Gaussian packet is almost identical to the delay time. Since the thesis ¹⁴ is not so readily available, several salient features of this work is highlighted here. First, the Green's function for the one dimensional equation for the DB structure is obtained. Excitation functions are chosen for various cases : specifying a spatial distribution at $t = 0$, or specifying a time function (usually a pulse at a given energy between $t = 0$ to T) at a given location such as $x = 0$, or $x = \text{center of the well}$, etc. Laplace transform is then used. The inverse transforms give the desired results. If one wants to calculate the charge inside the well at any given time for a particular distribution, it would be necessary to multiply $Q(t)$ for the charge by $n(\omega) - n'(\omega)$ and integrate over all ω , the energy, with n and n' given by the distribution functions on the inside and transmitted side of the DB respectively. $Q(t)$ confined within the system is obtained as a function of time by integrating $|\psi(t)|^2$ over both the well and the barrier regions. The decay time τ is defined by $Q(T + \tau) = Q(T)/e$, and the build-up time by $Q(\tau) = (1 - e^{-1}) Q_0$ where Q_0 is the steady state charge in the well. This definition is not unique particularly at energies away from the resonance, because the charge oscillates through the same value several times accept near resonance. Uniformly growing or decaying behavior of the charge only takes place near resonance! Instead of specifying the initial condition at the left side of the DB structure, we have also studied the build-up time and decay time for an excitation $\exp(-i\omega t)$ at a point within the well and calculate the steady state wavepacket. To our surprise, as the point of excitation moves towards the center of the well from the edge of the barrier, the resonance behavior gradually disappears. Note that, the resonance peak of the decay time and build-up time is broader than that of the Gaussian packet. Therefore, the

details of those cases are not quite the same, presumably precise results do depend on the form of the excitation. Although all these cases are similar: tunneling does slow down near resonance.

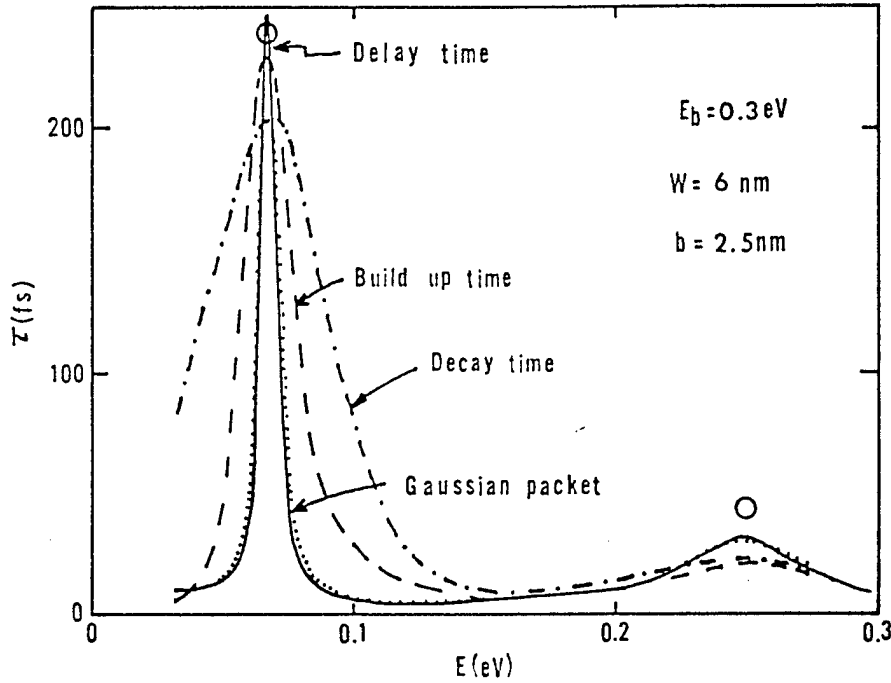


Fig. 1 Tunneling time calculated from the time dependent Schroedinger equation versus Energy For a double barrier structure with parameters given in the text. Note that the delay time is almost same as tunneling time for a Gaussian packet. The build up time, dashed; and the carrier decay time, dash-dot; inside the well, have broader resonances.

The delay time calculated from Eq.(1) is almost identical to the tunneling time for a Gaussian packet. Although tunneling time slows down near resonance, at the first resonance, the tunneling time is still less than one quarter of a ps, and 25 fs near the second resonance. Therefore, an ideal resonant tunneling device itself is very fast.

1.2. Capacitance of a Nanoscale Sphere

A classical capacitor stores charges, and the electrostatic energy is the only energy stored. However, electrons have kinetic energy even as standing waves confined inside a quantum well or quantum dot. We have calculated the quantum mechanical capacitance of a small sphere from the definition

$$E_2 - E_1 = e^2 / 2C_{\text{eff}} , \quad (2)$$

where E_1 and E_2 are the one- and two-electron ground state energies of a silicon sphere embedded in an amorphous silicon dioxide matrix.¹⁵ In our calculation, the electron-electron interaction and polarization effects are treated by perturbation; our result is valid for small spheres with radii between 1nm and 4nm. For large spheres, classical electrostatics is used. To our surprise, even the classical case has not been fully treated. Our results are useful for an understanding of transport measurements, such as resonant tunneling, because the voltages required to bring in additional electrons to the silicon particle are determined by the ground states, and the Coulomb energy involving the capacitance, known as Coulomb blockade.^{16,17} For optical response, excited states must also be included. Since we found that C_{eff} at 12nm approaches the classical value, approximately 10^{-18} F, we found that at 6nm and 3nm, C_{eff} is only one-half and one-third as large as the classical values, respectively. Likharev used a constant value for the capacitance in his Hamiltonian, which was alright as long as the size of the quantum dot is quite large.¹⁸

In brief, quantum mechanically an electron has energy in addition to the electrostatic energy even confined in a well. The energy of an electron is inversely proportional to the square of the dimension of confinement, therefore grows faster than the Coulomb energies. Consequently, C_{eff} decreases when the ground state energies dominate over the electrostatic energies. In principle, it should be possible to synthesize capacitor using this size effect. However, as we show here that appreciable decrease shows up only for particle size under 10nm. The fundamental understanding is actually more profound, the RC time constant in circuits should be broadened because in classical systems, charges can leak out only electrostatically, whereas quantum mechanically, an electron can also tunnel out of the confining barriers by virtue of its kinetic energy.

1.3. Dielectric Constant of Nanoscale Silicon Particle

Reduction of the static dielectric constant becomes significant as the size of the quantum confined systems, such as quantum dots and wires, approaches the nanometric range. A reduced static dielectric constant increases Coulomb interaction energy between electrons, holes, and ionized shallow impurities in quantum confined structures. The increase of the exciton binding energy significantly modifies the optical properties, and the increase of the shallow impurity binding energy may profoundly alter the transport, i.e., resulting in an intrinsic conduction even extrinsically doped. The size-dependent dielectric constant $\epsilon(a)$ was first derived using a modified Penn model taking into account the eigenstates of a sphere instead of the usual free electron energy-momentum relation.^{19,20} The effects of the reduction of dielectric constant in nanoscale silicon is presented by Tsu and Babic.²¹ Since then similar results were obtained by using far more sophisticated calculations.^{22,23} Strictly speaking, $\epsilon(q)$ should be used in the calculation of the screened shallow impurity potentials.^{24,25} However, it is a formidable task to contend with the electrostatic boundary conditions. These calculations become much more manageable if, instead of using $\epsilon(q)$, a constant but size-dependent dielectric constant $\epsilon(a)$ is used. Although this method is not rigorous, it provides an approximation that is suitable for calculations that involve the electrostatic boundary value problem at dielectric discontinuity.²⁶

The size-dependent $\epsilon(a)$ is given by²⁷

$$\epsilon(a) = 1 + (\epsilon_B - 1) / (1 + (\Delta E/E_g)^2), \quad (3)$$

and

$$\Delta E = \pi E_F / (k_F a), \quad (4)$$

where E_F and k_F are the energy and k vector at the Fermi level with the total number of the valence electrons, and E_g is taken as 4eV, the center of the ϵ_2 versus energy for silicon. Basically, confinement moves up the energies as well as discretizes the free electron E - k relations, resulting in a larger denominator in Eq.(3). In the Penn model, E_F is placed between two adjacent eigenstates. As the size is reduced, the adjacent states are separated more and more, resulting in a decrease in the dielectric constant. Figure 2 shows the calculated $\epsilon(a)$ versus a , the radius of a silicon sphere. Note that the comparison is almost perfect if $\epsilon_B = 11.3$, instead of 12, is used.

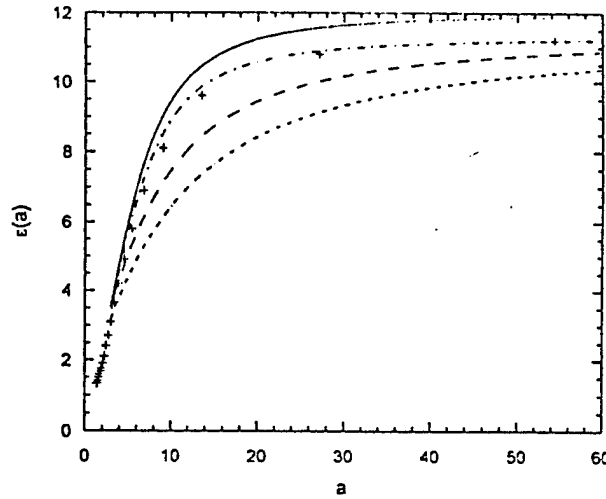


Fig. 2. $\epsilon(a)$ versus a of the silicon sphere in angstroms: the solid line is for $\epsilon_B = 12$ from Eq.(3); dash-dot is for $\epsilon_B = 11.3$; +++ depict $\epsilon(q)$ from Ref. 23 converted into $\epsilon(a)$ using $q = \pi/a$; the short-dash is from Ref. 20, and long-dash is from Ref. 21.

1.4. Doping of a Quantum Dot

As we discussed that the binding energies of shallow donors and acceptors should increase due to the decrease of the dielectric constant for small particles. It is simple to understand this increase because the Bohr radius is increased by a factor, the dielectric constant; and hydrogenic ground state is inversely proportional to the square of the static dielectric constant. At room temperature, for example, phosphorus doping has a binding energy slightly under twice $k_B T$, allowing extrinsic behavior at room temperatures. A significant increase of the binding energy would render a normally extrinsic material to be intrinsic. Moreover, electrochemical etching stops without a steady flow of holes to the surface. Therefore electrochemical etching without light in forming porous silicon is self-limiting,^{28,29} as particle size is reduced dopant binding energy increases, reducing the hole concentration.

From the discussions above, it seems that the binding energy of shallow dopants may be obtained using the Bohr expression. It turns out that realistically we need to imbed the nanoparticles in a matrix. The dielectric mismatch between the media results in induced charges at the interface. What we found for nanoscale size is that these induced effects are actually more important than purely dielectric constant effect. There are many such induced terms: in addition to the direct Coulomb term, there are the self-polarization between the electron and its image; the term between the electron and the induced polarization of the donor. Thus, we resorted to a variational calculation.³⁰ Since both the self-polarization and induced-polarization terms depend on $\epsilon_1 - \epsilon_2$, with 1 and 2 for the nanoparticle and the matrix respectively, the binding energy can be strongly affected by the sign of $\epsilon_1 - \epsilon_2$. Figure 3 shows the calculated binding energy versus the dot radius. For vacuum, at a radius of 2nm, the binding energy is 0.8eV, whereas immersing in water, the binding energy is reduced to 0.1eV, allowing some extrinsic conduction at room temperature!

Since doping is essential to the operation of semiconductor devices, and the trend of ever reducing the device size, the mechanism of extrinsic conduction governed by the size forms an important issue in device physics and device engineering. The dependence of the binding energy on the matrix was not envisioned before we started to calculate the binding energy. It turns out that this effect may be applied to carrier modulation : changing the carrier concentration by controlling the binding energy which in turn is controlled by the interface charge. Although the calculation applies to spheres, Ref. 30 also discussed the case of quantum wires.

This treatment leads to the situation that extrinsic conduction via shallow dopants as it stands in nanoscale semiconductors is diminishing for 1-2nm particle size. For this kind of size, conduction mechanisms resembles those governing coupled molecules. Therefore our treatment merely points to further studies.

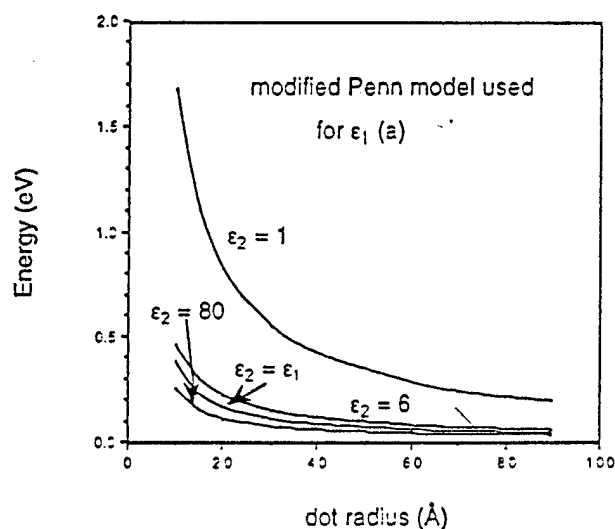


Fig. 3 Calculated binding energy versus the dot radius : for vacuum, top; matched dielectric constant; and water, bottom, 80 is reduced to 6 for the Helmholtz layer; from Ref.29.

2. Resonant Tunneling via Nanoscale Silicon Particles

Nicollian and I reasoned that if we could make the particles small enough, confinement would increase the energy separation to values allowing resonant tunneling at room temperature. I knew that more uniform particle size may be achieved by crystallization of silicon from the amorphous phase,^{31,4} and thin layer may result in even more uniform grain size due to experimental facts that silicon tends to crystallize in nearly spherical shape.³² Nanoscale silicon particles embedded in amorphous oxide circumvents the lack of a barrier for silicon, and most likely has less defects and unwanted strain, allowing the separation of energy states far exceeding $k_B T$. This project is certainly far more complex than most cases. Therefore, I want to describe the stages we ran into : several phases of the studies. For completeness sake, I want to summarize the preliminary stage involving the ARO contract DAALO3-90-G-0067/27443-EL.

2.1. Phase I

We instructed Ye, our postdoctoral fellow, to anneal the thin a-Si of thickness not more than 8nm in low pressure oxygen at 800-850°C. We knew that 950°C would have been better from defects point of view, nevertheless, a lower temperature was chosen, partly because most of my previous studies of the crystallization of silicon were at lower temperatures. A diode structure was fabricated with results reported in Ref. 4, where sharp conductance peaks were observed at reverse bias between 10-11 V. Figure 4, shows the schematic view of the diode structure. The μ c-layer is fabricated by post-annealing a thin amorphous silicon layer, in an oxygen-rich environment. Figure 5, taken from Ref. 5 is reproduced here for the convenience of the reader. Resonant tunneling diode, RTD, gives current peaks whenever the energy of the incident electron coincides with the eigenstates of the quantum system.² However, using a metal contact having a large Fermi energy, current steps instead of peaks should result at resonant.²⁰ The fabrication procedure were given to Chou⁷; when we, Nathan, Chou, and I were involved in a joint proposal to the Army Research Office. However, Ye convinced Nicollian and I that better, more repeatable, results require much thicker a-Si layer. At that point, I remembered my work at the Energy Conversion Devices on the crystallization of amorphous silicon and Ge with inhibiting layers. A thin layer of a-Ge sandwiched between two a-Si layers could not be crystallized at the T_c of a-Ge below 10nm thick, reaching almost the T_c of a-Si at 5nm

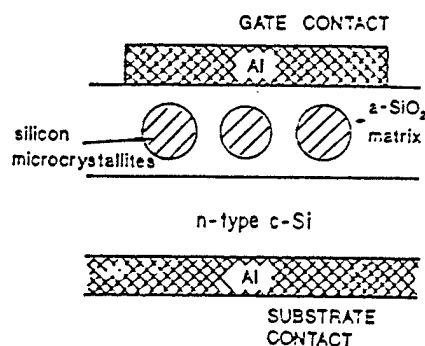


Fig. 4 A schematic diagram of the vs reverse diode structure

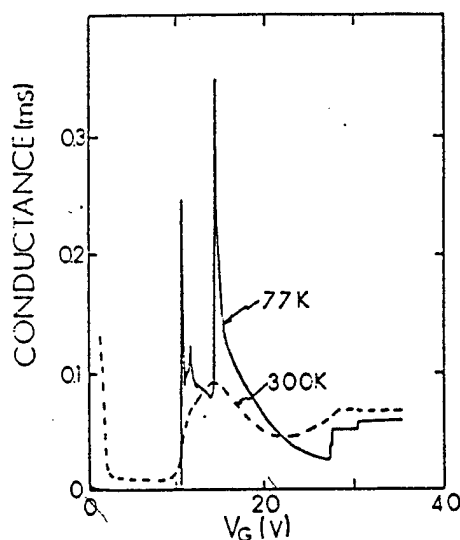


Fig. 5 Conductance bias at 77K and 300K

thickness. This work led to the Patent by Allred et al on the crystallization inhibition by constraining layers.³³ To crystallize thin a-Si sandwiched between oxide layers, it is necessary to anneal at a temperature above 1100°C. At such a high temperature other deleterious effects would have come into play. Thus we decided to anneal at 850°C with an increase of the a-Si thickness to 18nm. It is therefore quite obvious to us that Chou and Gordon⁷ most likely worked on a-Si instead of crystallized silicon particles! We discovered that the conductance peaks near 10V-11V reverse bias are very repeatable, but the structures above 20 volts bias usually are steps, having a pronounced hysteresis as shown in Fig.6 taken from the thesis of X.L.Li.³⁴ Note that there is a 0.2V shift. We found that about 1/30 of the applied voltage appears across the DB diode structure^{6,35} The actual hysteresis shift is about 7mV. Figure 7 shows another case having two groups of steps, having exceedingly large shift, almost 80mV across the DB! Number of steps going up is always the same as the number going down. This is very different from what was reported in Ref. 7. Hysteresis for peaks is almost unobservable, less than 100μV. We shall come back to this subject in the next section after we have discussed fully the electrical forming. Incidentally, whenever we observed non-reversible and non-repeatable structures in I-V such as that shown in Fig.2 of Ref. 7, we discarded the sample as bad sample, essentially amorphous, leading to breakdowns! On the other hand one can always produce breakdowns by going to extremely high bias voltage. We were quite bothered by the fact that there are too many structures than the number of quantum states anticipated. Nicollian started Li on an electrical forming procedure, hopefully can eliminate some of the unwanted structures. The rationale is that electrical forming is selective, capable of removing the amorphous tissue region either by crystallization or by "burning off", as well as removing the tiny crystallites in favor of larger ones. However, this forming procedure, improves things; but introduces more mysterious results.

These new features will be discussed in Phase II of the next section. What follows represent mostly work under this ARO contract.

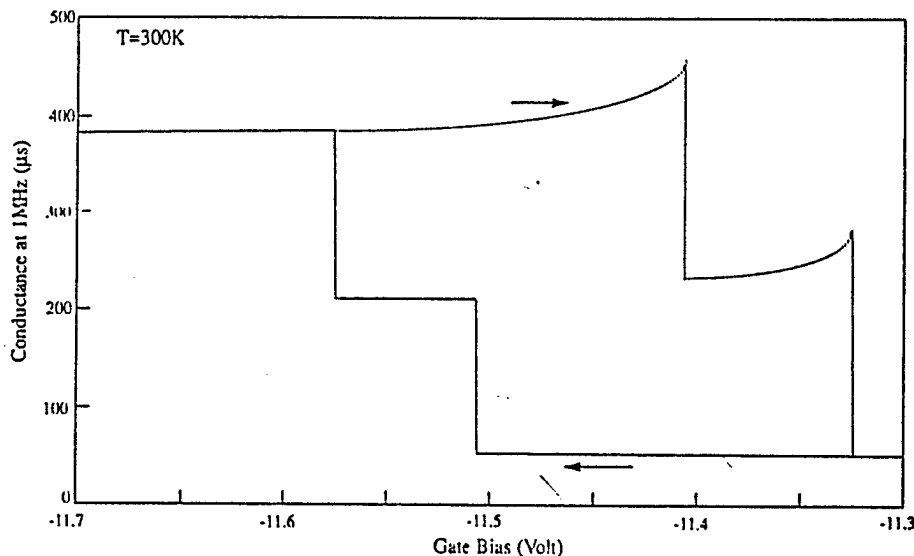


Fig. 6 Hysteresis effects taken from Ref. 34, showing a shift, 0.2V, corresponding to 80mV across the DB diode.

2.2. Phase II : With Electrical Forming

First of all, due to the presence of a Schottky barrier, approximately 0.6eV, the diode I-V shows the typical high current in the forward bias, and almost no current, except sharp structures in the reverse bias. Electrical forming is successful in producing almost complete reversibility and repeatability! However, as mentioned in the last section, new mysterious features showed up, slow conductance oscillation.³⁵ As we have mentioned that there are two types of conductance structures, peaks and steps. After introducing forming, we learned the nature of these two types. Forming was always performed in the forward bias for better control, and lower voltage so that to prevent avalanching. At a given applied voltage of typically 5V, slow scan gives rise to steps, and fast scan produces peaks. This was a breakthrough discovered by Li.³⁴ We can, for the first time control the type of structure! Our original assumption⁵ that steps are from 1-D like confinement and peaks for 3-D like confinement was basically sound. Slow scan supplies more thermal energy to the intergranular tissue, allowing the growth of larger crystals resulting in a quantum-well-like case because of wavefunction overlap, whereas fast scan produces smaller crystals with dot-like behavior. We have never observed the slow oscillation without forming, and whenever oscillation occurs, the base-line G-V is usually steps rather than peaks. Once we learned to control the peaks and steps, we discovered that slow oscillation always happens with step-like structures.³⁵ Actually, Li found out later that oscillation also was present with peaks, only that the oscillation is so fast that appeared to us as noise.³⁴ These peaks

are actually oscillation starting from given points on a step due to negative resistance. This is consistent with the slow hysteresis with steps and extremely fast hysteresis with peaks.

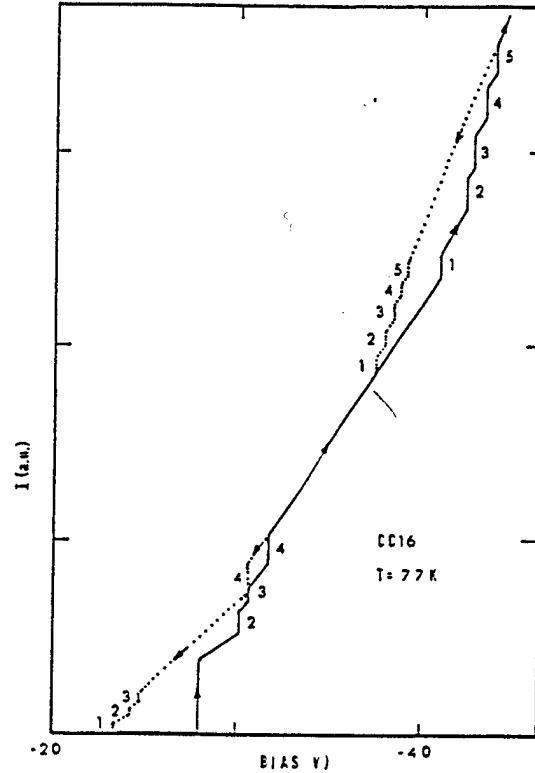


Fig. 7. Hysteresis from a sample showing two groups separated by 12V corresponding to 0.4V across the DB diode, close to the case using Eq.(6) below.

With a large Fermi surface of a metal, $G-V$ is proportional to the density of states in the quantum confined region, peaks for 3-D confinement, and steps for 1-D confinement. We reasoned that it is possible that electrical forming has "fused" the dots into an effective quantum wells by coupling these individual μ -crystallites. As we mentioned that these slow oscillations are so stable that persist a whole day. In addition to what were shown in Ref. 35, Fig. 8 shows a trace which has not been published thus far. As mentioned in Ref. 35, the on-time and off-time of the conductance can change drastically with a 1% change of the bias voltage. In order to better understand the arguments on the origin of the observed hysteresis and the slow oscillations, a brief discussion is presented on Coulomb blockade. The voltage required to aligned the metal contact with the n th quantum state is⁵

$$V_n = E_n / e + (e / C) n + e Q / C, \quad (5)$$

where E_n is the n th quantum state of the dot, C the capacitance of the dot, and Q representing charges trapped in localized defects. As long as we can assume that Q is constant for V_n and V_{n+1} , the adjacent peak should be separated by

$$\Delta V = (E_{n+1} - E_n) + e / C . \quad (6)$$

For a silicon particle of radius 5nm, the energy separation $E_2 - E_1$ is about 0.06eV, ⁴ C is about 0.6×10^{-18} F, e^2 / C is 0.35 eV, giving $\Delta V = 0.41$ V. With the factor of 30 we mentioned earlier, the separation in the measured should be about 12 V, what is shown in Fig. 7, the separation between the two groups. Therefore, we are quite sure the two groups represent tunneling through the first and the second quantum states.

Figure 8 shows the oscillatory G-V for a typical steps at -12.25V, top; and -12.36V, bottom. Note the drastic change in such a small difference in the applied voltage. Incidentally, these are totally repeatable, i.e. going from the top to the bottom and returning to the applied voltage of the top repeats the top trace!. In Ref. 35, it was assumed that some sort of mechanism similar to that proposed for the small MOSFET presented by Ralls et al ³⁶ may be applicable. The model does predict extremely slow period of oscillation. However other models seem to be also viable, capable of fitting the data well. At this point, I should emphasize that we do not have sufficient data to eliminate one or favoring the other.

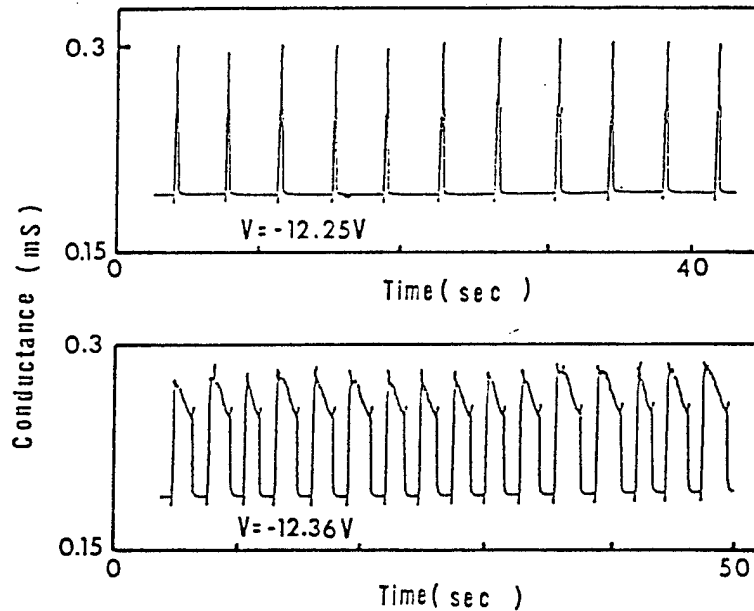


Fig. 8 A section of the G-V trace, of a typical step at two voltages.

We offered another explanation for the slow conductance oscillation : negative resistance due to avalanche in the substrate initiated by resonant tunneling. The details not only

explains the oscillation, but also predict the extremely small variation in the particle size as the origin of the "extra" conductance peaks.³⁷ The particle size determined for the best fit of the G-V data is in general agreement with the TEM determination of the $\mu\text{-Si}$ particle size, for example, 7nm for the former and 6 nm for the latter. (The size is less than half of the thickness of the a-Si layer, partly due to oxidization.) It should be noted that Chou and Gordon⁷ stated that they have observed negative resistance in one of their sample but failed to reproduce it in any ways later. First of all, one should not observe current peaks in resonant tunneling with metal contacts.²⁰ Thus, current peaks in their work, most likely is of the same origin : avalanche in the substrate! Incidentally, if Chou and Gordon had used the electrical forming in the forward direction having better control , perhaps they would have repeated their negative resistance results! However, they still would have to recognize that the negative resistance is real negative resistance, rather than NDC, negative differential conductance in conventional RTD.

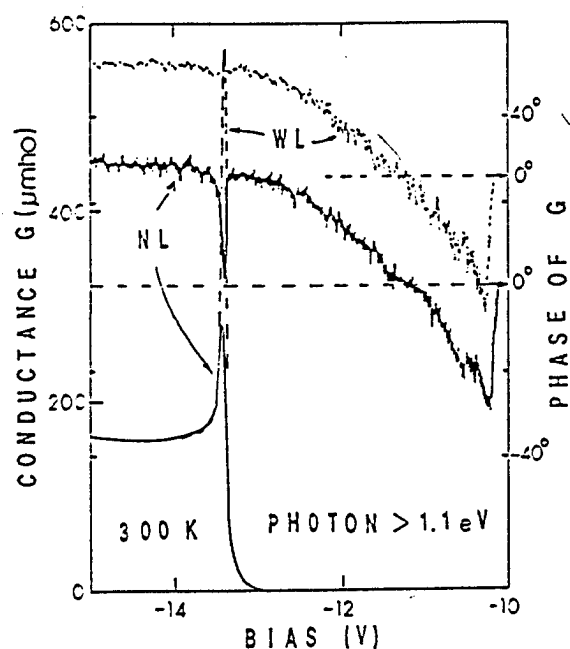


Fig. 9 Phase and conductance G vs. bias with and without illumination with light.

Another very interesting finding after forming is the observed light induced effects. Figure 9 shows the drastic sharpening of the conductance peak and the appearance of a sharp peak in C-V under illumination with photons at the band-gap energy of silicon,³⁸ we suggested that the enhancement with illumination is due to filling of traps from photo-generated carriers, and these measurements may be used to study traps in resonant tunneling. We have also replaced Al contact by polysilicon.³⁹ Results were disappointing because we did not succeed in

NDC. However, we found that usually with polysilicon contact, electrical forming seems less important.

2.3. Phase III : Thin oxide

We have studied identical diode without the thin a-Si layer followed by annealing, but with all other steps remaining the same. Bowhill⁴⁰ had found that it is possible to produce conductance structures somewhat similar to those at a bias of 20V or higher. The requirement is to apply a reverse bias voltage of more than 60V! After noisy conductance peaks appeared, more usual looking structures showed up during the retrace at a bias of 20-30V. The position is totally random, e.g. sometimes at 50V, sometimes at 70V. These structures, usually in the form of peaks, show no hysteresis, and is almost totally random. What is happening may be inadvertent forming in the reverse bias. It is important to point out that forming in the forward bias gives rise to much better control because at a forward bias of several volts, there is no avalanche instability to contend with. Nevertheless, we have also used electrical forming for the thin oxide case, the structures were still unrepeatable and becoming irreversible in few traces. We thus conclude that electrical forming of thin oxide may produce defects and even silicon precipitates with much more complex physical structures, leading to an unstable system due to complex couplings of these defects and precipitates.

2.4. A Brief Summary

This work has come to a pause or an end partly because we first lost the NSF support, and left with only the support of ARO. My colleague Ed Nicollan, unexpectedly passed away on December of 1995, which left me to deal with this extremely complex studies alone. There are other important factors that contributed a shift in propriety, the discovery of visible luminescence (supported by ONR) in a multilayer silicon based structure having many periods of thin silicon layers sandwiched between adsorbed oxygen,^{41,42} and the discovery of the epitaxially grown silicon beyond an adsorbed monolayer of oxygen^{43,8,9}, which allows the fabrication of epitaxial SOI and possible quantum devices.

A brief summary of results is listed :

(a) To improve repeatability, one needs to make sure that crystallization occurs. Since below a thickness of 20nm, it becomes much harder to crystallize, the thickness of the amorphous layer should be at least 20nm. And then, the particle size may be too big, from the mean-free-path point of view. Electrical forming improves repeatability because the process is selective. Then there is the issue due to a distribution of particle size. In a constrained case, the distribution is much smaller, however, the energy eigen- state is inversely proportional to the square of the size, and unwanted extra structures may limit the range of application, unless these extra features are intended. From engineering point of view, as long as these features are repeatable, one is able to design a system utilizing our system. The oscillation due to avalanche in the substrate presumably can be eliminated by reducing the thickness of the substrate, higher doping or by going to an entirely different device configuration such as the FET on SOI. However, there are

complex issues must be understood, for example, the role of traps and hysteresis, the charging effects, and the interface defects. At this stage, we think that oscillation may very well be due to both mechanisms,^{35,37} just as the two types of conductance structures. Inelastic tunneling dominates before the onset of resonant tunneling, which dominates the current. Resonant tunneling triggers many observed structures, including even breakdowns. On the other hand, irreversible breakdown is not an issue because it is an issue in all devices.

(b) The work has reached a point where larger resources are required to make significant progress. My priority has shifted towards other systems requiring small resources and having better chance for short-term returns : the epitaxial Si/O superlattice, which is presented in the next section. However, it should be recognized that breakdowns in oxide via tunneling through localized defects and/or precipitates might be of interest to those that work on the degradation of thin oxides.

3. Epitaxial Si/O Superlattice

It was proposed that in a Si/SiO₂ superlattice with SiO₂ no more than a couple of monolayers may serve as a strained layer barrier system for silicon.⁴⁴ After failing in several attempts, a new procedure was developed,⁴³ partially because we have developed a process to produce visible light by depositing the Si /adsorbed oxygen multilayer system on glass substrate,⁴¹ (Supported by ONR) In preparing the same structure on a silicon wafer for TEM, it was noted that the RHEED pattern may indicate crystalline even after the adsorption of a monolayer of disordered oxygen. We then launched⁴³ a new endeavor (In addition to our ARO contract, we were benefited by our collaboration with Nanodynamics under a BMDO Phase I, resulted in going to the University of Illinois for the initial experiments.) that became the precursor to our present effort in a variety of cases utilizing the fact : the silicon growth beyond an adsorbed oxygen is epitaxial. Epitaxy generally begins to recover in a thickness of the silicon growth exceeding 2nm.⁸ Figures 10 and 11, taken from Ref. 8 are presented here for the convenience of the reader.

Figure 10 shows the in-situ RHEED pattern during deposition. The 2x1 dimerization, the half order, is clearly shown in (a) from surface reconstruction of Si(100). Exposure to 10L (1 Langmuir is 10⁻⁸ Torr of Oxygen at 100 sec.) of oxygen at room temperature does not alter the 2x1 structure, until 1.1nm of Si is deposited, 0.03nm/s at 550°C, resulting in 3-D like pattern shown in (b). Repeating the process one more time does not change much as shown in (c). Finally, after 8nm Si, 0.04nm/s at 550°C, the 2-D pattern is fully restored shown in Fig.10 (d). This series of RHEED demonstrate that epitaxial growth is continued beyond the adsorbed oxygen layer. To fully recover the 2-D pattern for a four time repeated sequence with 10L oxygen exposure followed by 1.1nm of Si requires 12nm of silicon deposition. This indicates that there is a progressive deterioration. The maximum repeats we have done to date is nine.

Figure 11 shows a typical high resolution cross-section TEM lattice image with two 10L of adsorbed oxygen. The presence of clusters of oxygen with dimension approximately 3nm is evident. Note that there is no signs of disorder in the lattice image because the penetration of e-beam results in taking several layers with the silicon atoms in their proper lattice positions. We have found that the Si/O superlattice provides a surprisingly uniform electrical barrier of almost 0.5 eV, in spite of the nonuniformity shown in X-TEM. First of all if the clusters have "holes" of

dimension less than the de Broglie wavelength of the electrons, electrons cannot "leak out" through these small holes. It was pointed out that a smoothing effect can be caused by the local depletion due to the pinning of Fermi level by the defects such as the dangling bonds surrounding the oxygen clusters.⁴⁵ What is remarkable is the lack of stacking fault defects.

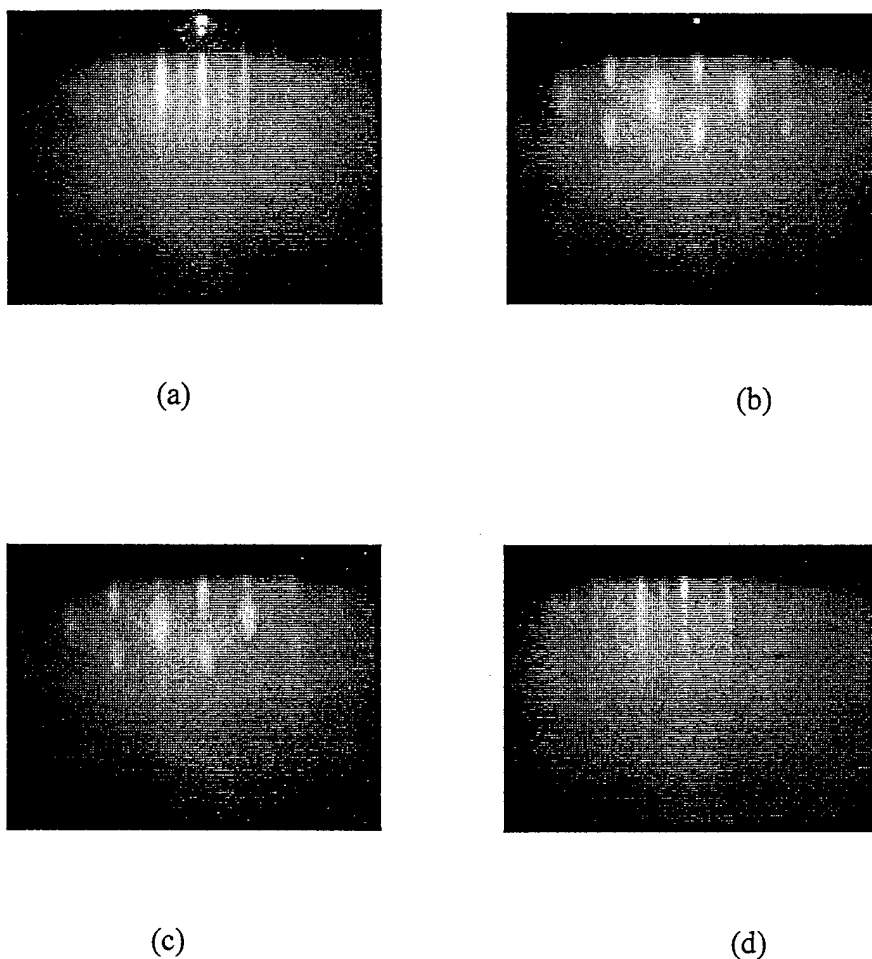


Fig. 10 RHEED of Si/O superlattice showing the re-establishment of epitaxy. The 1x2 reconstruction in (a) with 20nm Si buffer, 0.03nm/s at 550°C disappears after exposure of 10L of oxygen followed by 1.1nm of Si deposition, (b); and second repeat, (c). Full restoration is achieved after 8nm of silicon shown in (d).

Figure 12 shows I-V of a barrier consisting of a barrier with two 6L adsorption of oxygen separated by 1.1nm of silicon, compared with no barrier. The asymmetry of the I-V is mostly due to the Schottky barrier at the silicon / Al junction, as well as some possible

diffusion, because the layers deposited earlier have been subjected to 550°C more times than the later layers. By repeating the barriers, up to four times, we have reduced the current at -5V by 10^4 . At present we have initiated mobility measurements in the transverse plane. Preliminary results indicate that the mobility for Si beyond a barrier with 4 repeats as isolation, is much higher than a similar commercial SOI sample.

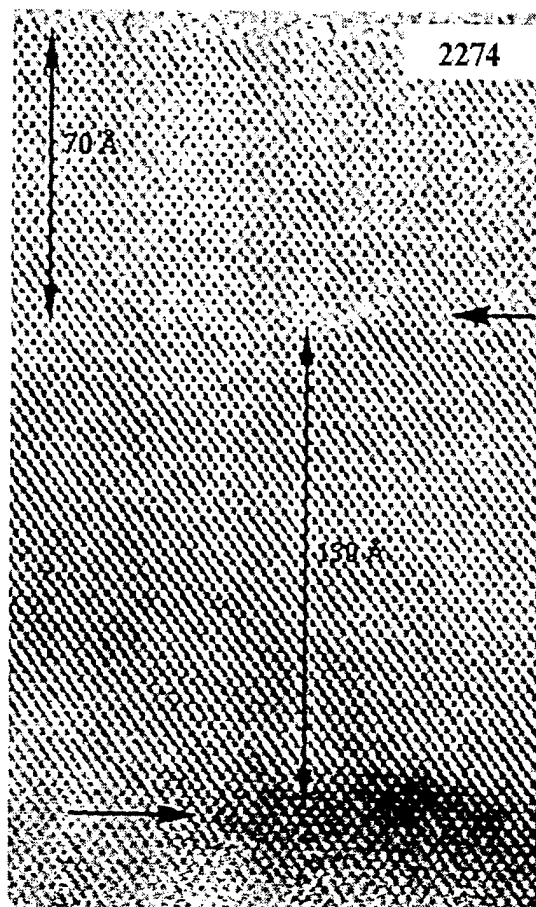


Figure 11 A typical high resolution cross-section TEM lattice image with 10L of exposed oxygen. Note that there is no stacking faults. The substrate / 15nm of buffer interface is marked by the left arrow, and the adsorbed oxygen, is between the 7nm of silicon on top, and the buffer layer.

A nine period superlattice shows electroluminescence with a broad peak centered at 2eV with spectrum extending to the blue.⁸ The EL device has been life tested up to six months with stable output. The efficiency is comparable to porous silicon devices, an efficiency of approximately 0.1%. Obviously increasing the oscillator in silicon by a small amount in

comparison to a direct bandgap semiconductor is not going to make a laser, the emission of light in this EL device can provide a start in photonic and electronic integration. The EL device is robust and fully compatible with the silicon processing technology.

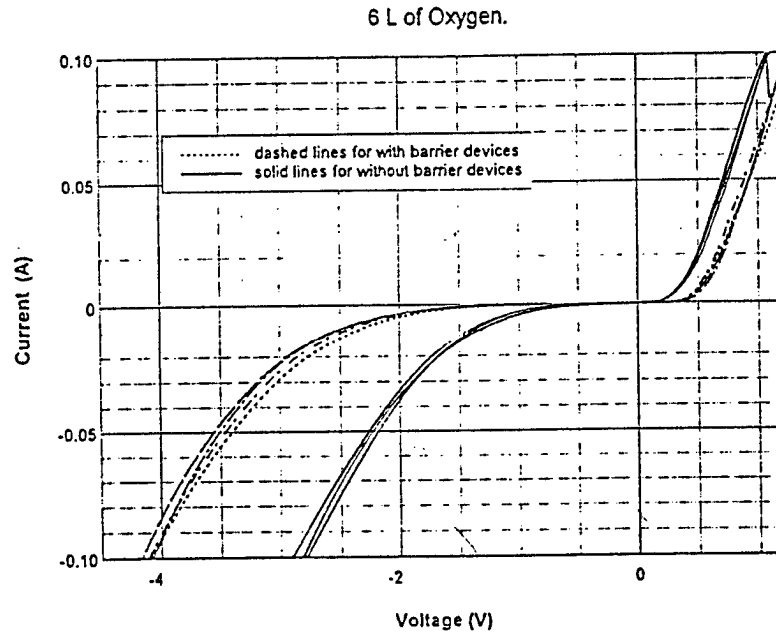


Fig. 12 Current vs Voltage for a barrier structure with and without the Si/O barrier. The asymmetry is mostly due to a Schottky barrier, Al contact / silicon.

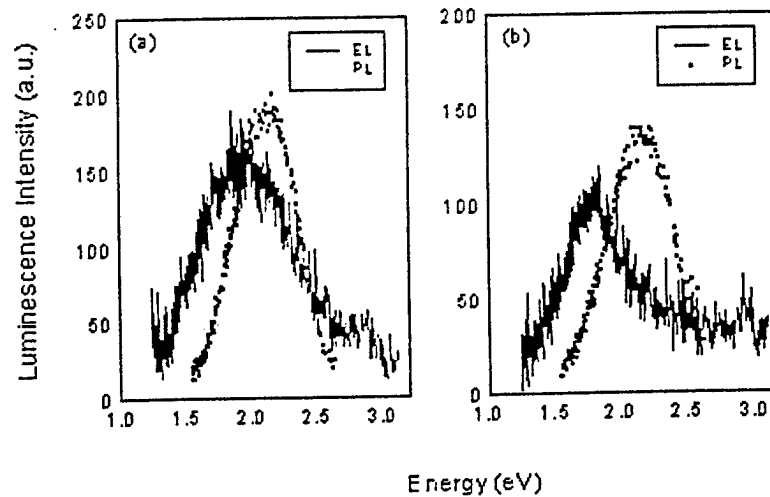


Fig.13 Electroluminescence spectra of a 9 period Si/O, EL, solid; and PL, dotted, measured at room temperature of (a) and (b) with reverse bias at $V = 14V$ and $20V$ respectively. PL was taken with the 457.9nm laser. Note that EL extends the spectra into higher photon energy .

As mentioned before, the possible near term application of the Si/O epitaxial barrier is to replace FETs on SOI,¹⁰ as a high speed and low power device. Therefore the Si/O superlattice is ready for further development in order to play a major role in the design of high speed transistors, as well as possible optoelectronic applications, a Si chip with both electronic and photonic components.

4. Conclusions

Speed and density go together : scaling down the device size leads to higher speed and density. How far can scaling go? Minimum operating voltages are set by the thermal voltage. Reducing size results ultimately to highfields beyond the breakdown. Besides, quantum effects will be reached at some point. These effects are not all desirable, for example, quantum interference is too size dependent, demanding unrealistic manufacturing tolerances. As the size approaches few nm, it is even impossible to dope due to the drastic increase in the binding energy of dopants. Classically, one talks about storing charges, as we have seen that quantum mechanically, one can only confine charges with a barrier. And electrons and holes confined in a barrier do leak out. Surely one can use thicker barrier to reduce tunneling, then, it is not possible to quickly remove the confined particle unless a large barrier-lowering field is applied. The problem with this scheme is that one needs to localize the applied field, otherwise many adjacent structures will be affected. What are needed are judicious applications of quantum effects far from the notion that quantum transistors must be better! Fortunately, what is focussed in this article is not about wide spread utilization of quantum confinement. Rather, in some specific applications, for example, (a) the epitaxial Si/O superlattice for replacing the SOI fabricated by ion-implantation, (b) fabrication of a RTD in silicon, (c) increasing the oscillator strength of silicon by quantum confinement for optoelectronic purposes, and (d) discretizing the I-V as resonant tunneling via nanoscale particles for multistage logic and functional devices. After stating all that, I am impelled to be optimistic that a totally new system fully utilizing the wave nature of quantum mechanics is right around the corner, waiting to be explored, even in silicon. The task at hand is huge, therefore, it is important to sort out those goals which can be successfully pursued with the available funding, to arrive at some consensus among the researchers for future endeavors.

Acknowledgements

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